MEMORY ARCHITECTURE FOR MICROMIRROR CELL

ABSTRACT

A one transistor one capacitor micromirror with DRAM memory cell built around a large polysilicon-to-substrate capacitor which is not susceptible to recombination of photo-generated carriers caused by illumination in the projector. This large polysilicon-to-substrate capacitor overshadows the much smaller inherent parallel depletion capacitance which is sensitive to light. The device is further 100% shielded from exposed light by metal layers and the address node is located under the center of the micromirror mirror to obtain maximum shielding of light for the smaller, light sensitive, depletion portion of the capacitance. As a result the micromirror of this invention can adequately hold the cell charge in excess of the device load time of 300 μSec even in extremely high brightness projector applications. This invention also provides a feature which automatically forces micromirror mirrors located over bad CMOS memory cell to the dark state, which is much less objectionable in most applications, thereby improving the overall effective processing yield.